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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,060	09/22/2003	Michel Harrand	S1022.81092US00	7268

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EXAMINER	
KIM, HONG CHONG	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,060	HARRAND ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-15,17 and 18* is/are rejected.

7)☒ Claim(s) *4,5 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/075,001.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-18 are presented for examination. This office action is in response to the application filed on 9/22/2003.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 9/22/2003. The information disclosed therein was considered.

Claim Objections

3. Claims 9-18 are objected to because of the following informalities: As to Claim 9, it appears that claim is subject to an undue breadth objection/rejection, since it is a single means claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 9-14, 17-18, 1-3, 7-8 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Keryvel et al. (Keryvel) US Patent No. 5,175,832.

As to claim 9, Keryvel discloses a fast random access DRAM memory (Fig.1) comprises a plurality of memory banks (Fig. 1 MM) accessible independently in read and write mode; means for comparing an address of a memory bank of the plurality of memory banks corresponding to a current request with addresses of memory banks of

the plurality of memory banks corresponding to N-1 previous requests, N being an integral number of cycles necessary to execute a request (col. 7 lines 20-26).

As to claim 10, Keryvel further discloses means for identifying the address of the memory bank corresponding to the current request (col. 7 lines 20-26).

As to claim 11, Keryvel further discloses means for, if the address of the memory bank corresponding to the current request is equal to an address of a memory bank corresponding to at least one of the N-1 previous requests, suspending and storing the current request until the at least one of the N-1 previous requests is executed, otherwise, executing it (col. 7 lines 20-26).

As to claim 12, Keryvel further discloses means for storing N requests following the current request, and, if execution of the current request is suspended, executing a following request of the N following requests corresponding to a memory bank having an address not equal to an address of a memory bank corresponding to the N-1 previous requests (col. 7 lines 20-26).

As to claim 13, Keryvel further discloses means for, if the executed request is a read request, arranging back the read information in the order of the executed read requests (col. 7 lines 20-26, shift register and n shift).

As to claim 14, Keryvel further discloses means for storing data read during the first M cycles of memory use; and means for providing an output datum, M cycles after each read request (col. 7 lines 20-26, shift register and n shift).

As to claim 17, Keryvel further discloses wherein the memory banks of the plurality of memory banks are distributed into sets accessible in parallel, whereby each set statistically only needs to process half of the requests (Fig. 2, upper and lower buses).

As to claim 18, Keryvel further discloses wherein the memory banks of the plurality of memory banks are distributed into several groups, the memory banks of a same group sharing a same bus, and wherein two requests can be simultaneously transmitted to two distinct groups (Fig. 2, upper and lower buses).

As to claim 1, Keryvel discloses a method of fast random access a management of a DRAM memory (Fig. 2), including the steps of dividing the memory into memory banks (Fig. 2 MM) accessible independently in read and write mode; identifying an address of a bank concerned by a current request; comparing the address of the bank concerned by the current request with addresses of N-1 banks previously requested, N being an integral number of cycles necessary to execute a request; and if the address of the bank concerned by the current request is equal to the an address of at least one of the N-1 banks previously requested, suspending and storing the current request until the previous request involving the same bank is executed, otherwise, executing it (col. 7 lines 20-26, shift register and n shift).

As to claim 2, Keryvel further discloses wherein the suspension operation includes stacking the requests in a first-in/first-out memory (col. 7 lines 20-26, shift register and n shift).

As to claim 3, Keryvel further discloses further including for the data reading, the steps of storing in an output FIFO register the data read during the first M cycles of memory use; and providing an output datum of the FIFO register, M cycles after each read request (col. 7 lines 20-26, shift register and n shift).

As to claim 7, Keryvel further discloses wherein the memory banks are distributed into sets accessible in parallel, whereby each set statistically only needs to process half of the requests (Fig. 2 upper and lower buses).

As to claim 8, Keryvel further discloses wherein the memory banks are distributed into several groups, the memory banks of a same group sharing the a same bus, and wherein two requests can be simultaneously transmitted to two distinct groups (Fig. 2 upper and lower buses).

As to claim 6, Keryvel discloses a method of fast random access management of a DRAM memory (Fig. 2), including the steps of: dividing the memory into memory banks (Fig. 2 MM) accessible independently in read and write mode; identifying an address of a bank concerned by a current request; comparing the address of the bank concerned by the current request with addresses of N-1 banks previously requested, N being an integral number of cycles necessary to execute a request, and if the address of the bank concerned by the current request is equal to an address of at least one of the N-1 banks previously requested, suspending and storing the current request until the previous request involving the same bank is executed, otherwise, executing it; storing N requests following the current request; if execution of the current request is

suspended, executing one of the N following requests not in conflict with a request being executed; and if the executed request is a read request, arranging back the read information in the order of the executed read requests (col. 7 lines 20-26, shift register and n shift).

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keryvel et al. (Keryvel) US Patent No. 5,175,832 in view of Eto, JP 03183094.

As to claim 15, Keryvel discloses the invention as claimed above, however, Keryvel does not specifically disclose discloses means for performing a refresh operation comprising refreshing the plurality of memory banks line by line and bank by bank; and means for comparing an address of a memory bank to be refreshed with addresses of memory banks corresponding to N-1 ongoing requests and addresses of memory banks corresponding to N following requests, and delaying the refresh operation if the address of the memory bank to be refreshed equals an address of at least one of the memory banks corresponding to the N-1 ongoing requests or the N following requests.

Eto discloses means for performing a refresh operation comprising refreshing (abstract) the plurality of memory banks line by line and bank by bank; and means for comparing an address of a memory bank to be refreshed with addresses of memory

banks corresponding to N-1 ongoing requests and addresses of memory banks corresponding to N following requests, and delaying the refresh operation if the address of the memory bank to be refreshed equals an address of at least one of the memory banks corresponding to the N-1 ongoing requests or the N following requests providing the data from the shared memory in response to the request before all read-only copies of the data retained by other requesters have been invalidated (abstract) for the purpose of improving the throughput (abstract).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate discloses means for performing a refresh operation comprising refreshing the plurality of memory banks line by line and bank by bank; and means for comparing an address of a memory bank to be refreshed (col. 10 lines 18-34) with addresses of memory banks corresponding to N-1 ongoing requests and addresses of memory banks corresponding to N following requests, and delaying the refresh operation if the address of the memory bank to be refreshed equals an address of at least one of the memory banks corresponding to the N-1 ongoing requests or the N following requests as taught by Eto into the system of Keryvel for the advantages stated above.

6. Claims 9-14, 18, 1-3, 8, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,870,572 ("Garcia").

As to claim 9, Garcia, in column 19, lines 45-65 and column 21, line 50 through column 22, line 45, discloses a fast random access DRAM memory accessible independently in read and write mode (for example, Fig. 3B); means for comparing an address of a memory bank of the plurality of memory banks corresponding to a current request with addresses of memory banks of the plurality of memory banks

corresponding to previous requests (inherent in column 19, lines 52-55 and column 22, lines 28-34).

However, Garcia does not disclose N-1 previous requests, N being an integral number of cycles necessary to execute a request.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a queue size of N-1, N being an integral number of cycles necessary to execute a request, in the system of Garcia, since only ordinary skill in the art is involved in determining an optimum size for the input queue.

As to claim 10, Garcia further discloses means for identifying the address of the memory bank corresponding to the current request (inherent in column 19, lines 52-55 and column 22, lines 28-34).

As to claim 11, Garcia further discloses means for, if the address of the memory bank corresponding to the current request is equal to an address of a memory bank corresponding to at least one of the N-1 previous requests, suspending and storing the current request until the at least one of the N-1 previous requests is executed, otherwise, executing it (inherent in column 19, lines 52-55 and column 22, lines 28-34).

As to claim 12, Garcia further discloses means for storing N requests following the current request, and, if execution of the current request is suspended, executing a following request of the N following requests corresponding to a memory bank having an address not equal to an address of a memory bank corresponding to the N-1 previous requests (inherent in column 19, lines 52-55 and column 22, lines 28-34).

As to claim 13, Garcia further discloses means for, if the executed request is a read request, arranging back the read information in the order of the executed read requests (for example, input queue 46 in Fig. 4).

As to claim 14, Garcia further discloses means for storing data read during the first M cycles of memory use(44 in Fig. 32); and means for providing an output datum, M cycles after each read request (DOUT of 44 in Fig. 32).

As to claim 18, Garcia in Fig. 2, further discloses wherein the memory banks of the plurality of memory banks are distributed into several groups (memory cards 26), the memory banks of a same group sharing a same bus, and wherein two requests can be simultaneously transmitted to two distinct groups (via global bus 24 and arbiter 36).

As to claim 1, Garcia, in column 19, lines 45-65 and column 21, line 50 through column 22, line 45, discloses a method of fast random access management of a DRAM memory, including the steps of: dividing the memory into memory banks accessible independently in read and write mode (for example, Fig. 3B); identifying an address of a bank concerned by the current request; comparing the address of the bank concerned by the current request with addresses of previous requests (inherent in column 19, lines 52-55 and column 22, lines 28-34); and if the address of the bank concerned by the current request is equal to an address of at least one of the previous requested, suspending and storing (in the input queue 46) the current request until the previous request involving the same bank is executed (column 22, lines 28-34), otherwise, executing it.

However, Garcia does not disclose N-1 previous requests, N being an integral number of cycles necessary to execute a request.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a queue size of N-1, N being an integral number of cycles necessary to execute a request, in the method of Garcia, since only ordinary skill in the art is involved in determining an optimum size for the input queue.

As to claim 2, Garcia further discloses that the suspension operation includes stacking the request in a memory of first-in/first-out (for example, input queue 46 in Fig. 4).

As to claim 3, Garcia further discloses for the data reading, the steps of: storing in an output FIFO register the data read during the first M cycles of memory use (44 in Fig. 32); and providing an output datum of the FIFO register, M cycles after each read request (DOUT of 44 in Fig. 32).

As to claim 8, Garcia, in Fig. 2, further discloses that the memory banks are distributed into several groups (memory cards 26), the memory banks of a same group sharing the same bus (26a), and wherein two requests can be simultaneously transmitted to two distinct groups (via global bus 24
and arbiter 36).

As to claim 6, Garcia, in column 19, lines 45-65 and column 21, line 50 through column 22, line 45, discloses a method of fast random access management of a DRAM memory, including the steps of: dividing the memory into memory banks accessible

independently in read and write mode (for example, Fig. 3B); identifying an address of a bank concerned by the current request; comparing the address of the bank concerned by the current request with addresses of previously requested and if the address of the bank concerned by the current request is equal to an address of at least one of the previously requested, suspending and storing (in the input queue 46) the current request until the previous request involving the same bank is executed (column 22, lines 28-34), otherwise, executing it; storing requests following the current request; if execution of the current request is suspended, executing one of the following requests not in conflict with a request being executed; and if the executed request is a read request, arranging back the read information in the order of the executed read requests.

However, Garcia does not disclose N-1 previous requests, N being an integral number of cycles necessary to execute a request.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a queue size of N-1, N being an integral number of cycles necessary to execute a request, in the method of Garcia, since only ordinary skill in the art is involved in determining an optimum size for the input queue.

Allowable Subject Matter

Claims 4-5 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
571-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
April 28, 2006